SDLS090 – OCTOBER 1976 – REVISED MARCH 1988

- **Contains Eight Flip-Flops With Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

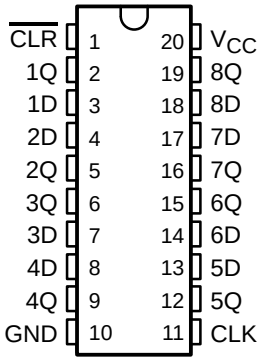
description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

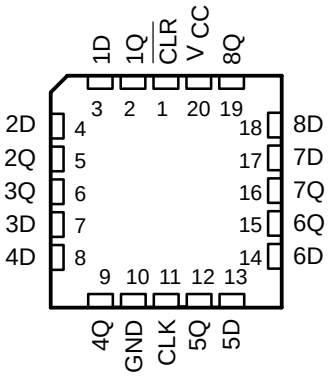
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect ar the output.

These flip-flops are guaranteed to respond to clock frequencies ranging form 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the ′273 and 10 milliwatts for the ′LS273.

SN54273, SN74LS273 . . . J OR W PACKAGE
SN74273 . . . N PACKAGE
SN74LS273 . . . DW OR N PACKAGE
(TOP VIEW)



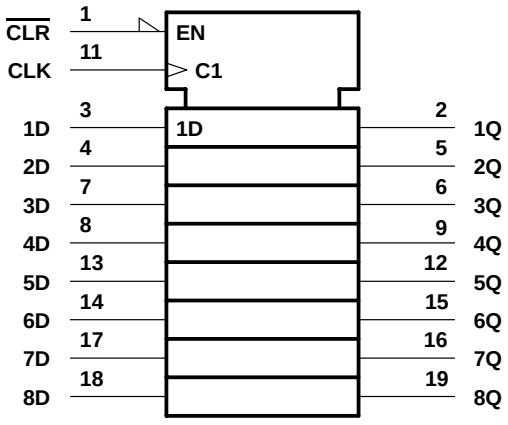
SN54LS273 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

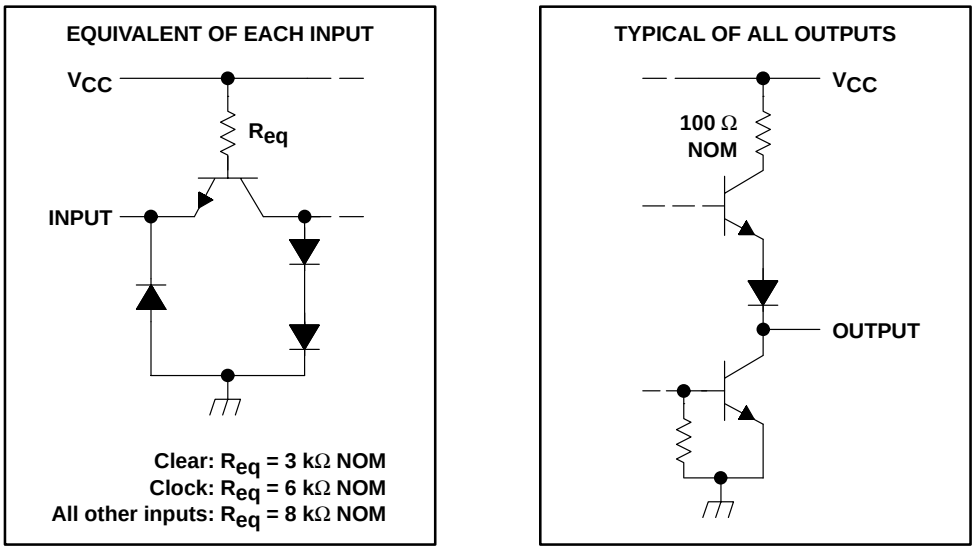
logic symbol†



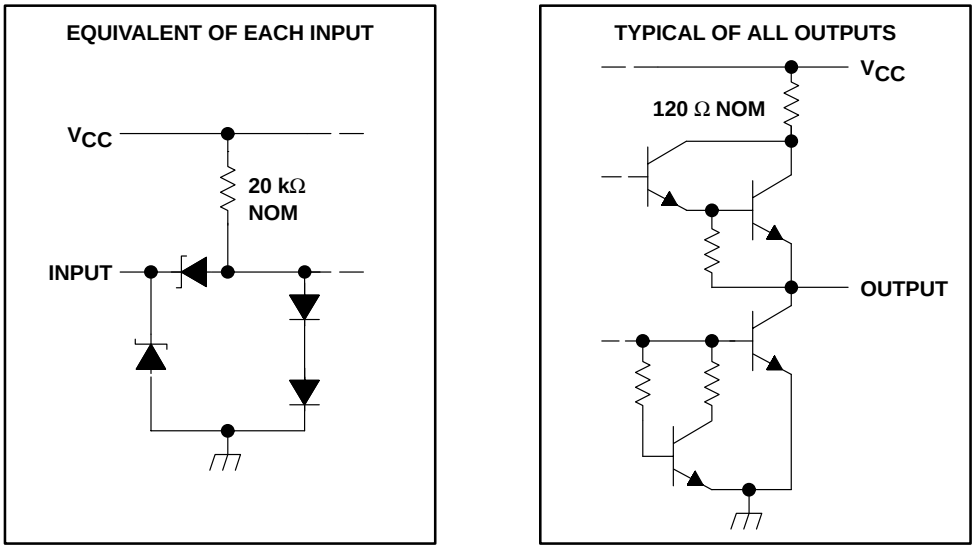
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, N, and W packages.

schematics of inputs and outputs

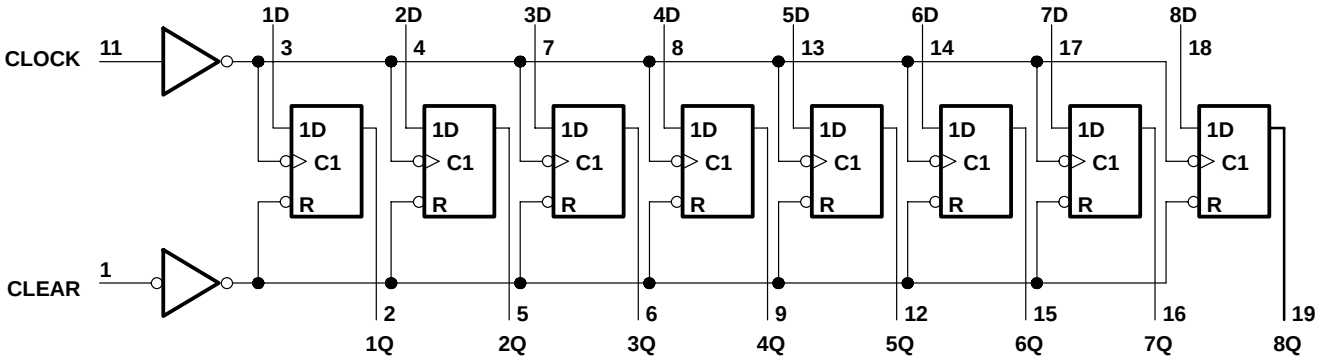
′273



′LS273



logic diagram (positive logic)



Pin numbers shown are for the DW, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54273 . . . . . –55°C to 125°C
SN74273 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54273			SN74273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–800			–800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		16.5			16.5			ns
Setup time, t_{su}	Data input	20↑			20↑			ns
	Clear inactive state	25↑			25↑			
Data hold time, t_h		5↑			5↑			ns
Operating free-air temperature, T_A		–55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = –12 mA			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = –800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = 16 mA			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Clear	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		Clock or D					40	
I_{IL}	Low-level input current	Clear	V_{CC} = MAX,	V_I = 0.4 V			–3.2	mA
		Clock or D					–1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		–18		–57	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		62	94	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range, T_A: SN54LS273 . . . . . −55°C to 125°C
SN74LS273 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS273			SN74LS273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20↑			20↑			ns
	Clear inactive state	25↑			25↑			
Data hold time, t_h		5↑			5↑			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS273			SN74LS273			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = –400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				–0.4			–0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			17	27		17	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			18	27	ns

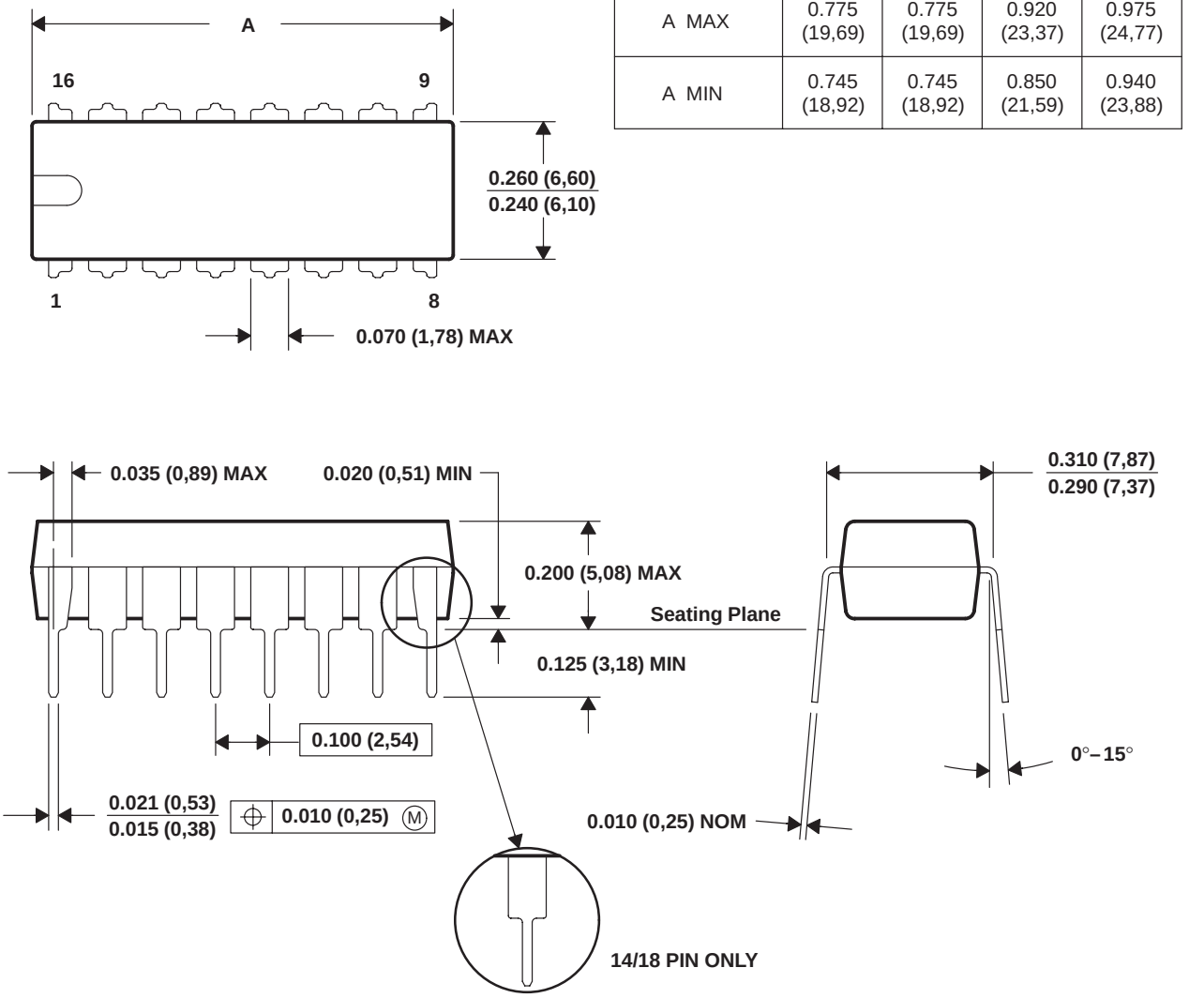
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

MPDI002A – JANUARY 1995 – REVISED OCTOBER 1995

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).