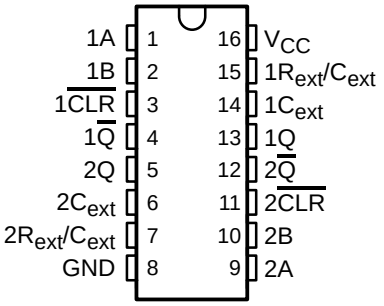
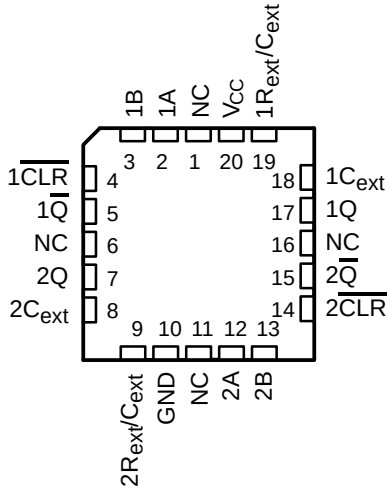
- **Dual Versions of Highly Stable SN54121 and SN74121 One Shots on a Monolithic Chip**
- **SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121 and SN74121 One Shots**
- **Pinout Is Identical to the SN54123, SN74123, SN54LS123, SN74LS123**
- **Overriding Clear Terminates Output Pulse**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK) and Flat Packs (W), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

TYPE	TYPICAL POWER DISSIPATION (mW)	MAXIMUM OUTPUT PULSE LENGTH (s)
SN54221	130	21
SN74221	130	28
SN54LS221	23	49
SN74LS221	23	70

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221 . . . N PACKAGE
SN74LS221 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS221 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′221 and ′LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the ′121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 V/s, providing the circuit with excellent noise immunity of typically 1.2 V. A high immunity to V_{CC} noise of typically 1.5 V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse length can be varied from 35 ns to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 ns is achieved which can be used as a dc-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse-width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability is only limited by the accuracy of external timing components.

description (continued)

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(out) = C_{ext}R_{ext}\ In2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ can be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution for the ′221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the ′221 are shown in Figures 3 and 4, respectively.

Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the ′221 or ′LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}; however, the polarity of the capacitor will have to be changed.

The SN54221 and SN54LS221 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74221 and SN74LS221 are characterized for operation from 0°C to 70°C.

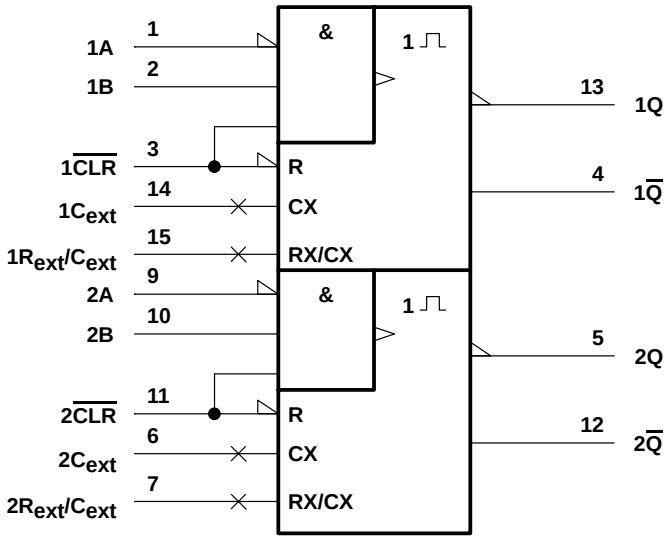
FUNCTION TABLE
(each monostable multivibrator)

INPUTS			OUTPUTS	
$\overline{CLR}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍ ‡	⎎ ‡
H	↓	H	⎍ ‡	⎎ ‡
↑†	L	H	⎍ ‡	⎎ ‡

† This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either A high or B low while $\overline{CLR}$ is inactive (high).

‡ Pulsed-output patterns are tested during AC switching at 25°C with R_{ext} = 2 kΩ, and C_{ext} = 80 pF.

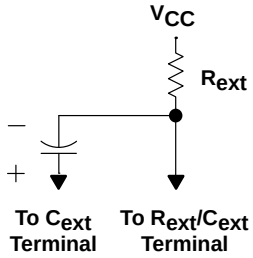
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

timing component connections

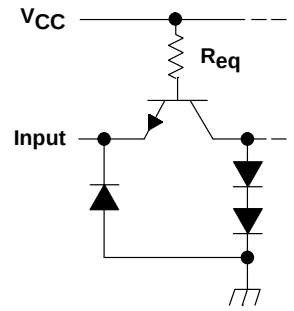


NOTE: Due to the internal circuit, the R_{ext}/C_{ext} terminal will never be more positive than the C_{ext} terminal.

schematics of inputs and outputs

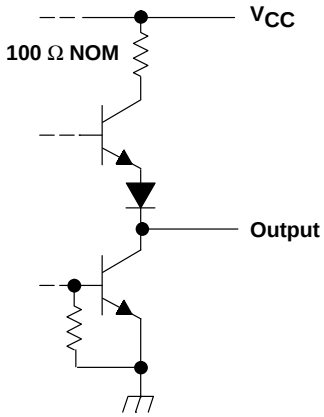
SN54/74221

EQUIVALENT OF EACH INPUT



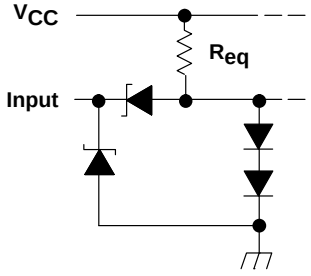
Input $\overline{A}$: R_{eq} = 4 kΩ NOM
Input B, $\overline{CLR}$: R_{eq} = 2 kΩ NOM

TYPICAL OF ALL OUTPUTS



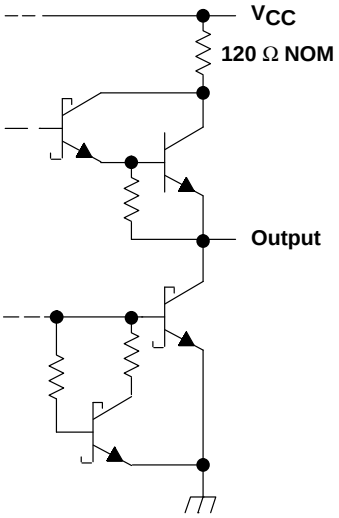
SN54/74LS221

EQUIVALENT OF EACH INPUT



Input A: R_{eq} = 25 kΩ NOM
Input B: R_{eq} = 15.4 kΩ NOM
$\overline{CLR}$: R_{eq} = 12.5 kΩ NOM

TYPICAL OF ALL OUTPUTS



recommended operating conditions

			SN54221			SN74221			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage at A		2			2			V
V_{IL}	Low-level input voltage at A				0.8			0.8	V
I_{OH}	High-level output current				– 800			– 800	μA
I_{OL}	Low-level output current				16			16	mA
$\Delta v/\Delta t$	Rise or fall of input pulse rate	Schmitt-input B	1			1			V/s
		Logic-input A	1			1			V/μs
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54221			SN74221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive going threshold voltage at B	V_{CC} = MIN			1.55	2		1.55	2	V
V_{T-}	Negative going threshold voltage at B	V_{CC} = MIN		0.8	1.35		0.8	1.35		V
V_{IK}		V_{CC} = MIN,	I_I = –12 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = – 800 μA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	Input A	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
	Input B, $\overline{CLR}$					80			80	
I_{IL}	Input A	V_{CC} = MAX,	V_I = 0.4 V			–1.6			–1.6	mA
	Input B, $\overline{CLR}$					–3.2			–3.2	
I_{OS}§		V_{CC} = MAX		–20		–55	–18		–55	mA
I_{CC}	Quiescent	V_{CC} = MAX			26	50		26	50	mA
	Triggered				46	80		46	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			SN54221		SN74221		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	A or B, $t_{w(in)}$	50		50		ns
		$\overline{CLR}$, $t_{w(clear)}$	20		20		
t_{su}	Inactive-state setup time†	$\overline{CLR}$	15		15		ns
R_{ext}	External timing resistance		1.4	30	1.4	40	kΩ
C_{ext}	External timing capacitance		0	1000	0	1000	μF
	Output duty cycle	R_{ext} = 2 kΩ		67%		67%	
		R_{ext} = MAX R_{ext}		90%		90%	

† Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 400 Ω, T_A = 25°C			UNIT
				SN54221, SN74221			
				MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B				35	55	
t_{PHL}	A	$\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ		50	80	ns
	B				40	65	
t_{PHL}	$\overline{CLR}$	Q	C_{ext} = 80 pF, R_{ext} = 2 kΩ			27	ns
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ			40	ns
t_w	A or B	Q or $\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	110	150	ns
			C_{ext} = 0, R_{ext} = 2 kΩ	17	30	50	
			C_{ext} = 100 pF, R_{ext} = 10 kΩ	650	700	750	
			C_{ext} = 1 μF, R_{ext} = 10 kΩ	6.5	7	7.5	ms

recommended operating conditions

			SN54LS221			SN74LS221			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage at A		2			2			V
V_{IL}	Low-level input voltage at A				0.7			0.8	V
I_{OH}	High-level output current				– 400			– 400	μA
I_{OL}	Low-level output current				4			8	mA
$\Delta v/\Delta t$	Rise or fall of input pulse rate	Schmitt-input B	1			1			V/s
		Logic-input A	1			1			V/μs
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive going threshold voltage at B	V_{CC} = MIN			1	2		1	2	V
V_{T-}	Negative going threshold voltage at B	V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}		V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = – 400 μA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Input A	V_{CC} = MAX,	V_I = 0.4 V			–0.4			–0.4	mA
	Input B, $\overline{CLR}$					–0.8			–0.8	
I_{OS}§		V_{CC} = MAX		–20		–100	–20		–100	mA
I_{CC}	Quiescent	V_{CC} = MAX			4.7	11		4.7	11	mA
	Triggered				19	27		19	27	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

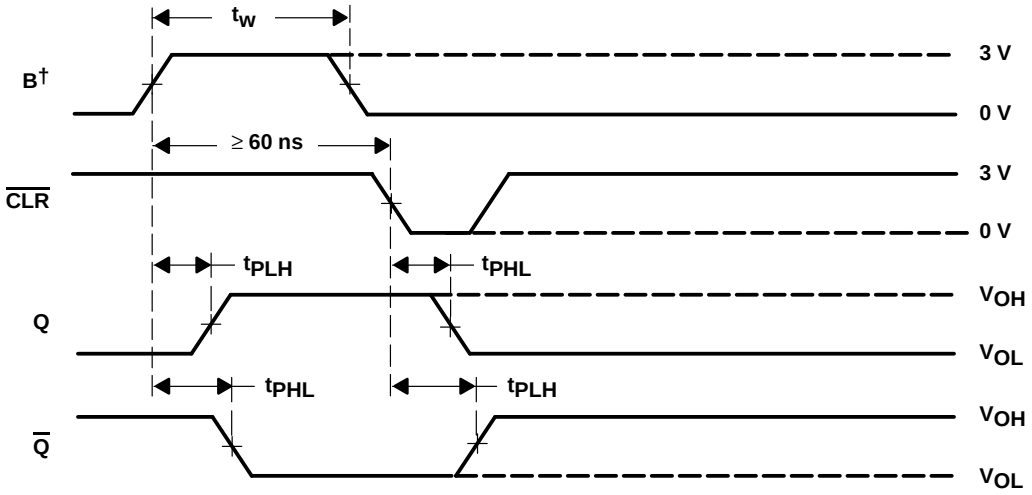
			SN54LS221		SN74LS221		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	A or B, $t_{w(in)}$	50		50		ns
		$\overline{CLR}$, $t_{w(clear)}$	40		40		
t_{su}	Inactive-state setup time†	$\overline{CLR}$	15		15		ns
R_{ext}	External timing resistance		1.4	70	1.4	100	kΩ
C_{ext}	External timing capacitance		0	1000	0	1000	μF
	Output duty cycle	R_T = 2 kΩ		50%		50%	
		R_T = MAX R_{ext}		90%		90%	

† Inactive-state setup time is also referred to as recovery time.

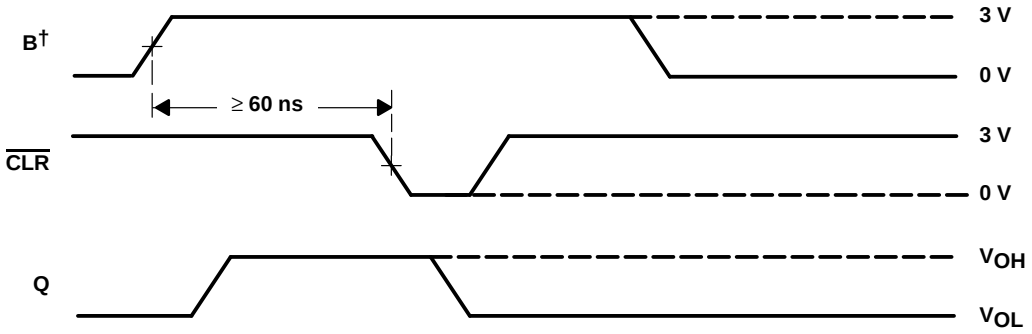
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			UNIT
				SN54LS221 SN74LS221			
				MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B				35	55	
t_{PHL}	A	$\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ		50	80	ns
	B				40	65	
t_{PHL}	$\overline{CLR}$	Q	C_{ext} = 80 pF, R_{ext} = 2 kΩ		35	55	ns
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ		44	65	ns
t_w	A or B	Q or $\overline{Q}$	C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	120	150	ns
			C_{ext} = 0, R_{ext} = 2 kΩ	20	47	70	
			C_{ext} = 100 pF, R_{ext} = 10 kΩ	670	740	810	
			C_{ext} = 1 μF, R_{ext} = 10 kΩ	6	6.9	7.5	ms

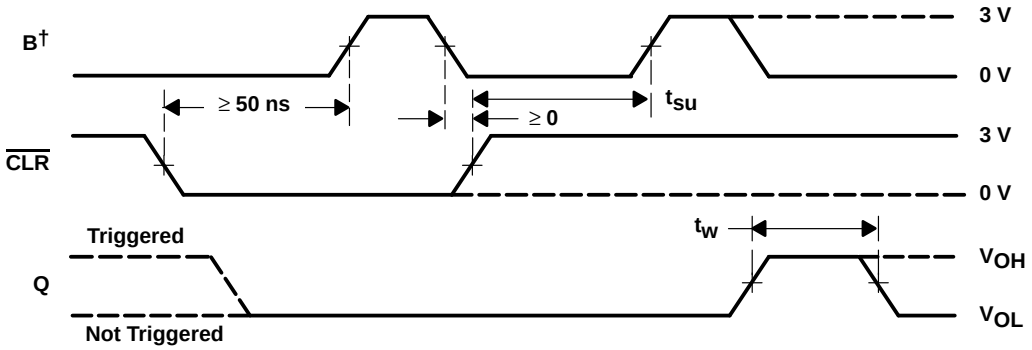
PARAMETER MEASUREMENT INFORMATION



CONDITION 1: TRIGGER FROM B, THEN $\overline{CLR}$



CONDITION 2: TRIGGER FROM B, THEN $\overline{CLR}$

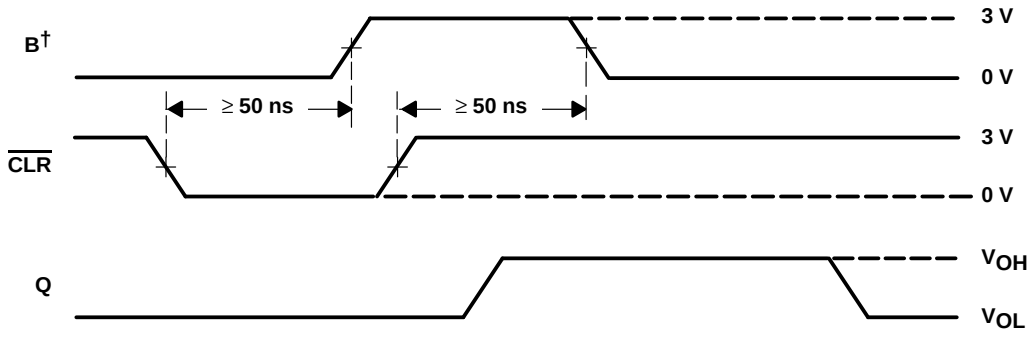


CONDITION 3: $\overline{CLR}$ OVERRIDING B, THEN TRIGGER FROM B

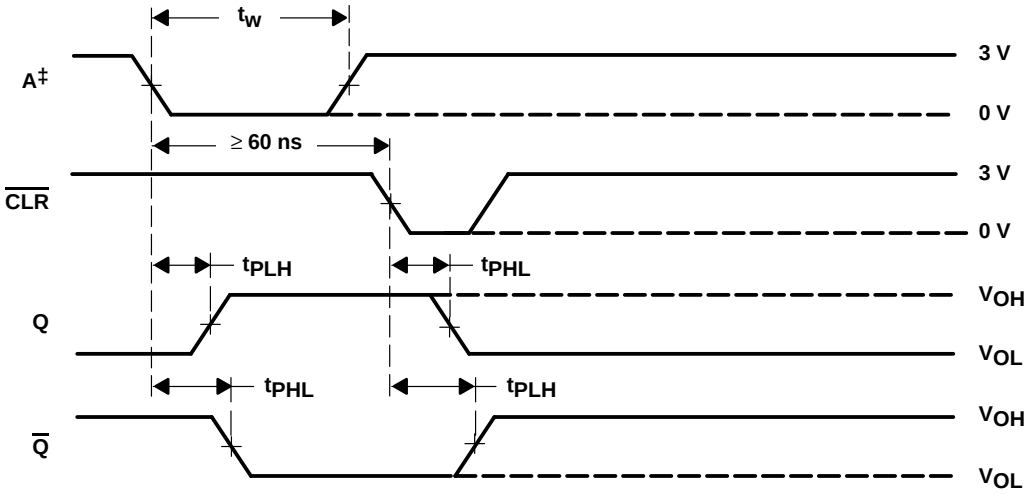
† A is low.

Figure 1. Switching Characteristics

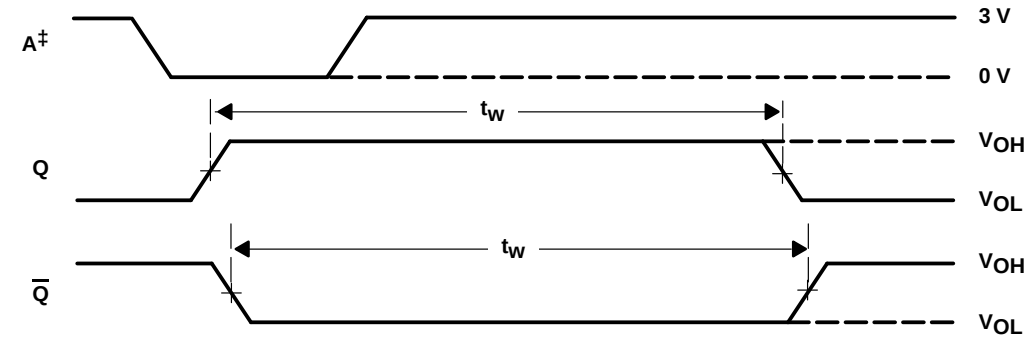
PARAMETER MEASUREMENT INFORMATION



CONDITION 4: TRIGGERING FROM POSITIVE TRANSITION OF $\overline{CLR}$



CONDITION 5: TRIGGER FROM A, THEN $\overline{CLR}$



CONDITION 6: TRIGGER FROM A

† A is low.
‡ B and $\overline{CLR}$ are high.

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\Omega$; for SN54/74221, $t_r \le 7$ ns, $t_f \le 7$ ns, for SN54/74LS221, $t_r \le 15$ ns, $t_f \le 6$ ns.
B. All measurements are made between the 1.5-V points of the indicated transitions for the SN54/74221 or between the 1.3-V points for the SN54/74LS221.

Figure 1. Switching Characteristics (Continued)

TYPICAL CHARACTERISTICS (SN54/74221 ONLY)†

DISTRIBUTION OF UNITS FOR OUTPUT PULSE

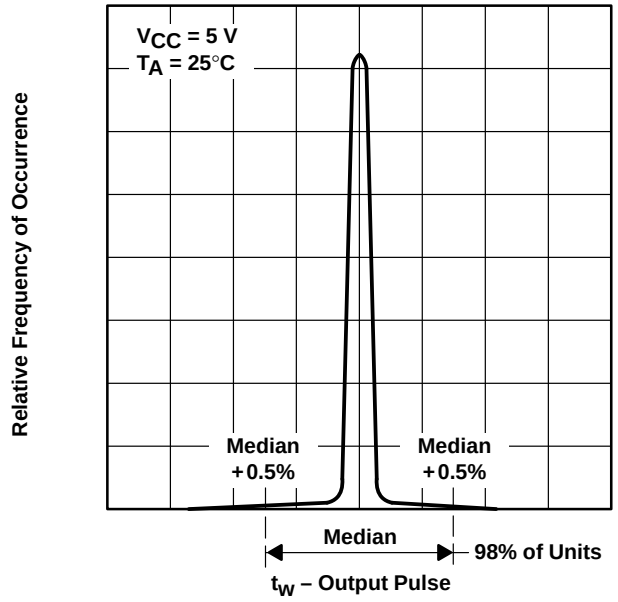


Figure 2

VARIATION IN OUTPUT PULSE vs SUPPLY VOLTAGE

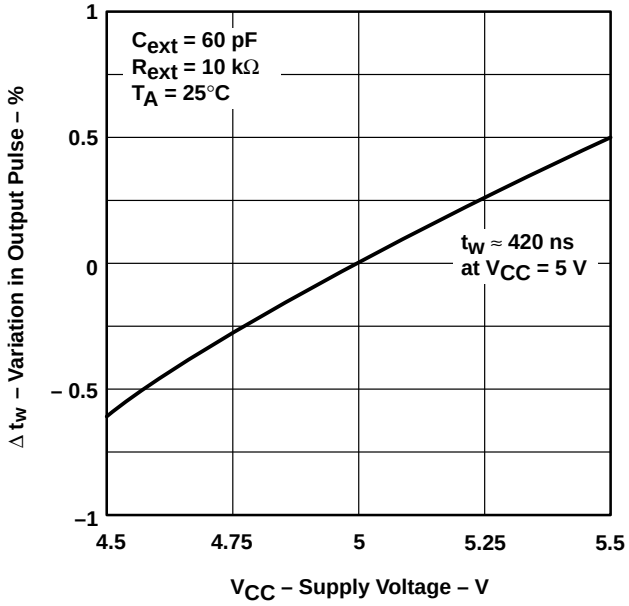


Figure 3

VARIATION IN OUTPUT PULSE vs FREE-AIR TEMPERATURE

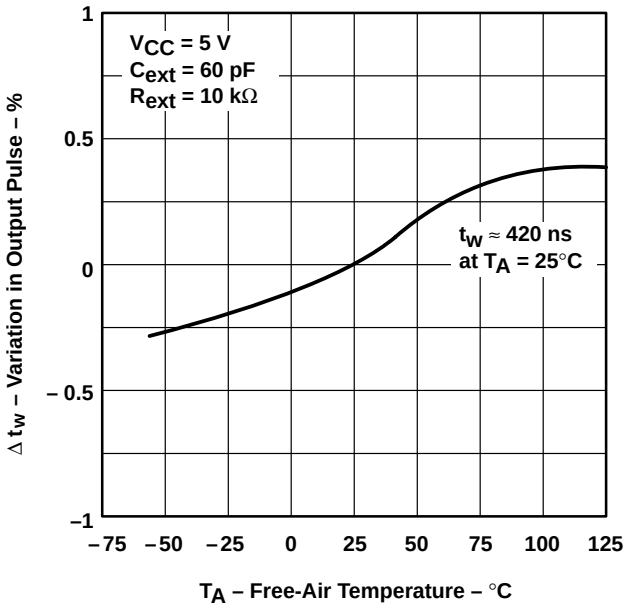


Figure 4

OUTPUT PULSE vs TIMING RESISTOR VALUE

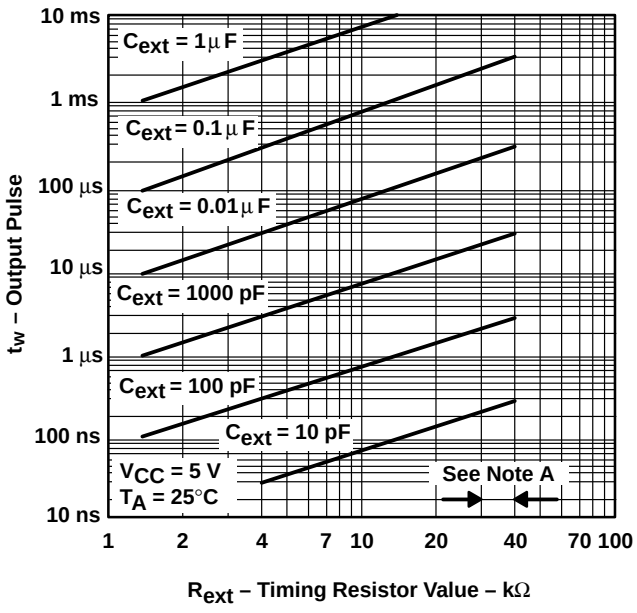


Figure 5

† Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.
NOTE A: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

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