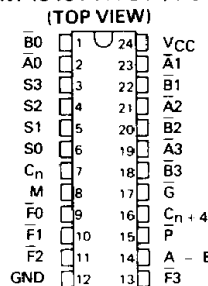


# TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

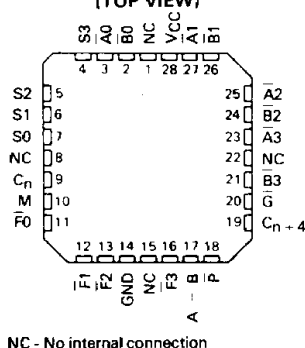
DECEMBER 1972 — REVISED DECEMBER 1983

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

SN54181, SN54LS181, SN54S181 ... J OR W PACKAGE  
SN74181 ... J OR N PACKAGE  
SN74LS181, SN74S181 ... DW, J OR N PACKAGE



SN54LS181, SN54S181 ... FK PACKAGE  
SN74LS181, SN74S181 ... FN PACKAGE



TYPICAL ADDITION TIMES

| NUMBER OF BITS | ADDITION TIMES      |                       |                       | PACKAGE COUNT           |                             | CARRY METHOD BETWEEN ALU's |
|----------------|---------------------|-----------------------|-----------------------|-------------------------|-----------------------------|----------------------------|
|                | USING '181 AND '182 | USING 'LS181 AND '182 | USING 'S181 AND 'S182 | ARITHMETIC/ LOGIC UNITS | LOOK-AHEAD CARRY GENERATORS |                            |
| 1 to 4         | 24 ns               | 24 ns                 | 11 ns                 | 1                       |                             | NONE                       |
| 5 to 8         | 36 ns               | 40 ns                 | 18 ns                 | 2                       |                             | RIPPLE                     |
| 9 to 16        | 36 ns               | 44 ns                 | 19 ns                 | 3 or 4                  | 1                           | FULL LOOK-AHEAD            |
| 17 to 64       | 60 ns               | 68 ns                 | 28 ns                 | 5 to 16                 | 2 to 5                      | FULL LOOK-AHEAD            |

## description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input ( $C_n$ ) and a ripple-carry output ( $C_{n+4}$ ) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

## PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TTL DEVICES

# TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## description (continued)

The '181, 'LS181, and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

| PIN NUMBER                 | 2              | 1              | 23             | 22             | 21             | 20             | 19             | 18             | 9              | 10             | 11             | 13             | 7              | 16               | 15        | 17        |
|----------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------|-----------|-----------|
| Active-low data (Table 1)  | $\bar{A}_0$    | $\bar{B}_0$    | $\bar{A}_1$    | $\bar{B}_1$    | $\bar{A}_2$    | $\bar{B}_2$    | $\bar{A}_3$    | $\bar{B}_3$    | $\bar{F}_0$    | $\bar{F}_1$    | $\bar{F}_2$    | $\bar{F}_3$    | $C_n$          | $C_{n+4}$        | $\bar{P}$ | $\bar{G}$ |
| Active-high data (Table 2) | A <sub>0</sub> | B <sub>0</sub> | A <sub>1</sub> | B <sub>1</sub> | A <sub>2</sub> | B <sub>2</sub> | A <sub>3</sub> | B <sub>3</sub> | F <sub>0</sub> | F <sub>1</sub> | F <sub>2</sub> | F <sub>3</sub> | C <sub>n</sub> | C <sub>n+4</sub> | X         | Y         |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is  $A-B-1$ , which requires an end-around or forced carry to provide  $A-B$ .

The '181, 'LS181, or 'S181 can also be utilized as a comparator. The  $A = B$  output is internally decoded from the function outputs ( $F_0, F_1, F_2, F_3$ ) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ( $A = B$ ). The ALU must be in the subtract mode with  $C_n = H$  when performing this comparison. The  $A = B$  output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( $C_{n+4}$ ) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs  $S_3, S_2, S_1, S_0$  at L, H, H, L, respectively.

| INPUT $C_n$ | OUTPUT $C_{n+4}$ | ACTIVE-LOW DATA<br>(FIGURE 1) | ACTIVE-HIGH DATA<br>(FIGURE 2) |
|-------------|------------------|-------------------------------|--------------------------------|
| H           | H                | $A \geq B$                    | $A \leq B$                     |
| H           | L                | $A < B$                       | $A > B$                        |
| L           | H                | $A > B$                       | $A < B$                        |
| L           | L                | $A \leq B$                    | $A \geq B$                     |

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs ( $S_0, S_1, S_2, S_3$ ) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ; Series 74, 74LS, and 74S devices are characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

## signal designations

The '181, 'LS181, and 'S181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (O) and the bars over the terminal letter symbols (e.g.,  $\bar{C}$ ) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at  $\bar{C}$  means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

**TYPES SN54181, SN54LS181, SN54S181,  
SN74181, SN74LS181, SN74S181  
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

signal designations (continued)

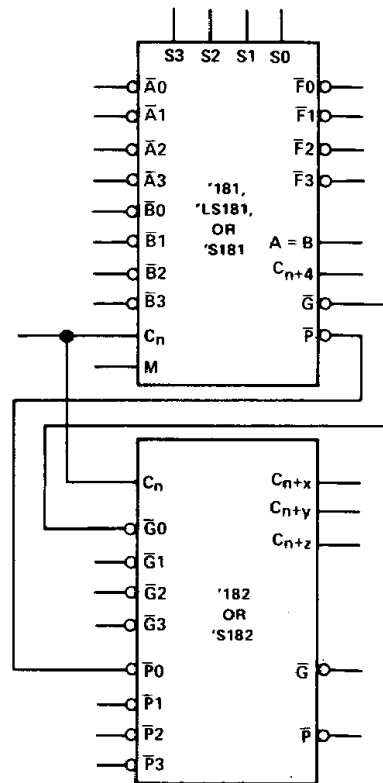


FIGURE 1

TABLE 1

| SELECTION |    |    |    | ACTIVE-LOW DATA             |                                           |                                                           |
|-----------|----|----|----|-----------------------------|-------------------------------------------|-----------------------------------------------------------|
|           |    |    |    | M = H<br>LOGIC<br>FUNCTIONS | M = L; ARITHMETIC OPERATIONS              |                                                           |
| S3        | S2 | S1 | S0 |                             | Cn = L<br>(no carry)                      | Cn = H<br>(with carry)                                    |
| L         | L  | L  | L  | $F = \overline{A}$          | $F = A \text{ MINUS } 1$                  | $F = A$                                                   |
| L         | L  | L  | H  | $F = \overline{AB}$         | $F = AB \text{ MINUS } 1$                 | $F = AB$                                                  |
| L         | L  | H  | L  | $F = \overline{A + B}$      | $F = \overline{AB} \text{ MINUS } 1$      | $F = \overline{AB}$                                       |
| L         | L  | H  | H  | $F = 1$                     | $F = \text{MINUS } 1 \text{ (2's COMP)}$  | $F = \text{ZERO}$                                         |
| L         | H  | L  | L  | $F = \overline{A + B}$      | $F = A \text{ PLUS } (A + B)$             | $F = A \text{ PLUS } (A + \overline{B}) \text{ PLUS } 1$  |
| L         | H  | L  | H  | $F = \overline{B}$          | $F = AB \text{ PLUS } (A + \overline{B})$ | $F = AB \text{ PLUS } (A + \overline{B}) \text{ PLUS } 1$ |
| L         | H  | H  | L  | $F = A \oplus B$            | $F = A \text{ MINUS } B \text{ MINUS } 1$ | $F = A \text{ MINUS } B$                                  |
| L         | H  | H  | H  | $F = A + \overline{B}$      | $F = A + \overline{B}$                    | $F = (A + \overline{B}) \text{ PLUS } 1$                  |
| H         | L  | L  | L  | $F = \overline{AB}$         | $F = A \text{ PLUS } (A + B)$             | $F = A \text{ PLUS } (A + B) \text{ PLUS } 1$             |
| H         | L  | L  | H  | $F = A \oplus B$            | $F = A \text{ PLUS } B$                   | $F = A \text{ PLUS } B \text{ PLUS } 1$                   |
| H         | L  | H  | L  | $F = B$                     | $F = \overline{AB} \text{ PLUS } (A + B)$ | $F = \overline{AB} \text{ PLUS } (A + B) \text{ PLUS } 1$ |
| H         | L  | H  | H  | $F = A + B$                 | $F = (A + B)$                             | $F = (A + B) \text{ PLUS } 1$                             |
| H         | H  | L  | L  | $F = 0$                     | $F = A$                                   | $F = A \text{ PLUS } A \text{ PLUS } 1$                   |
| H         | H  | L  | H  | $F = \overline{AB}$         | $F = AB \text{ PLUS } A$                  | $F = AB \text{ PLUS } A \text{ PLUS } 1$                  |
| H         | H  | H  | L  | $F = AB$                    | $F = \overline{AB} \text{ PLUS } A$       | $F = \overline{AB} \text{ PLUS } A \text{ PLUS } 1$       |
| H         | H  | H  | H  | $F = A$                     | $F = A$                                   | $F = A \text{ PLUS } 1$                                   |

**TYPES SN54181, SN54LS181, SN54S181,  
SN74181, SN74LS181, SN74S181  
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

signal designations (continued)

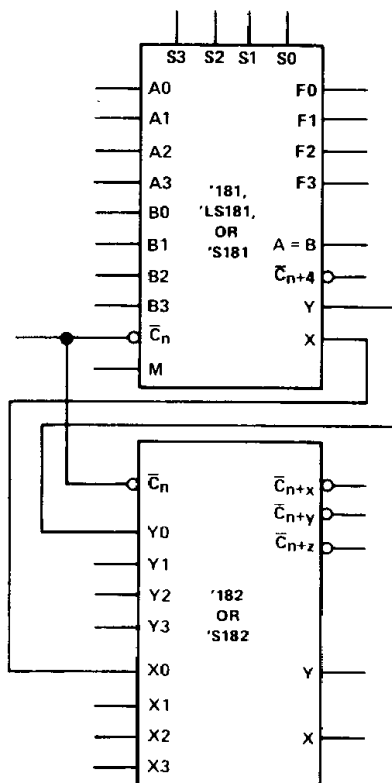


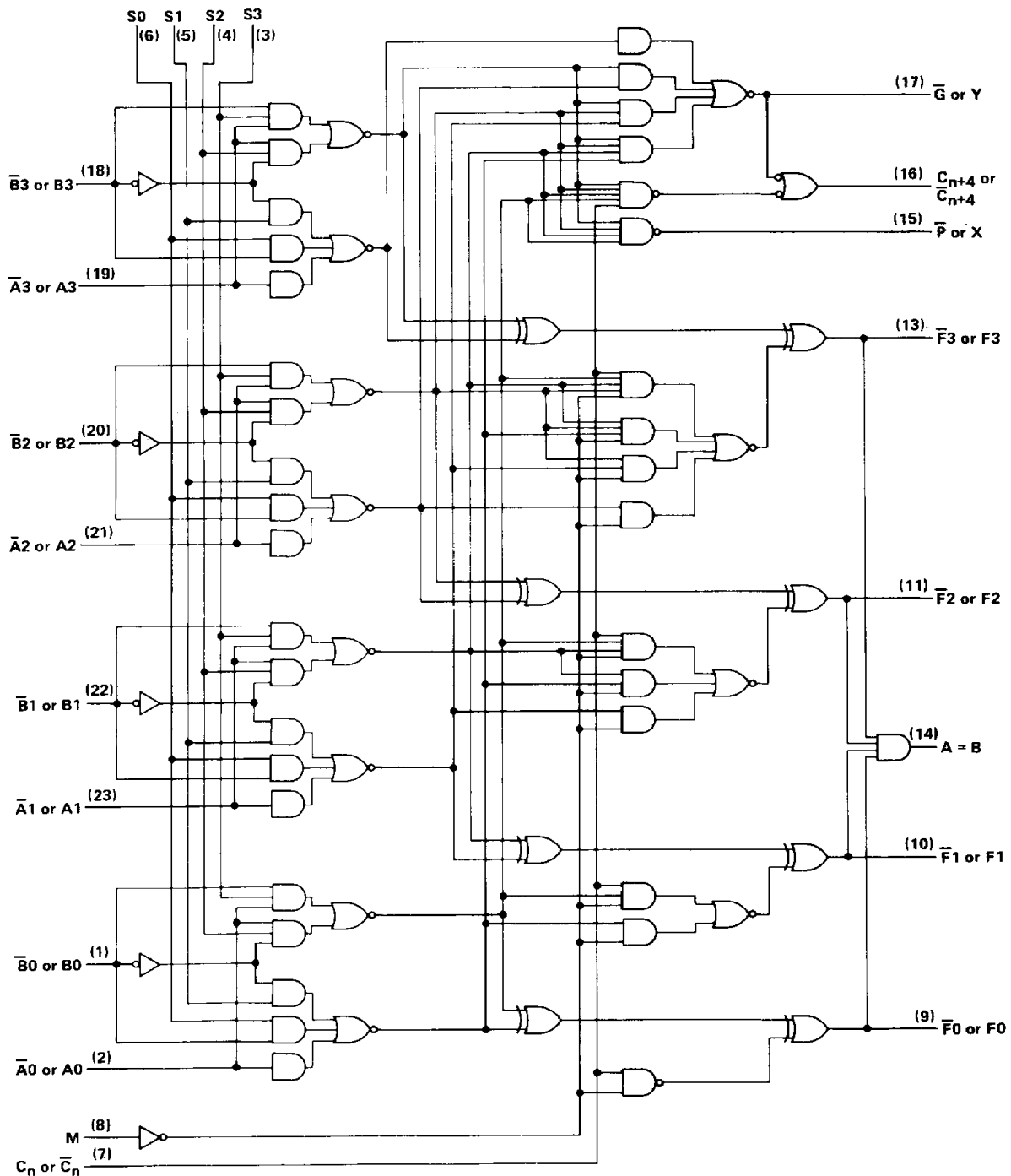
FIGURE 2

TABLE 2

| SELECTION |    |    |    |  | ACTIVE-HIGH DATA       |                                           |                                                           |
|-----------|----|----|----|--|------------------------|-------------------------------------------|-----------------------------------------------------------|
|           |    |    |    |  | M = H                  | M = L; ARITHMETIC OPERATIONS              |                                                           |
|           |    |    |    |  | LOGIC FUNCTIONS        | C <sub>n</sub> = H<br>(no carry)          | C <sub>n</sub> = L<br>(with carry)                        |
| S3        | S2 | S1 | S0 |  |                        |                                           |                                                           |
| L         | L  | L  | L  |  | $F = \overline{A}$     | $F = A$                                   | $F = A \text{ PLUS } 1$                                   |
| L         | L  | L  | H  |  | $F = \overline{A + B}$ | $F = A + B$                               | $F = (A + B) \text{ PLUS } 1$                             |
| L         | L  | H  | L  |  | $F = \overline{AB}$    | $F = A + \overline{B}$                    | $F = (A + \overline{B}) \text{ PLUS } 1$                  |
| L         | L  | H  | H  |  | $F = 0$                | $F = \text{MINUS } 1 \text{ (2's COMPL)}$ | $F = \text{ZERO}$                                         |
| L         | H  | L  | L  |  | $F = \overline{AB}$    | $F = A \text{ PLUS } \overline{AB}$       | $F = A \text{ PLUS } \overline{AB} \text{ PLUS } 1$       |
| L         | H  | L  | H  |  | $F = \overline{B}$     | $F = (A + B) \text{ PLUS } \overline{AB}$ | $F = (A + B) \text{ PLUS } \overline{AB} \text{ PLUS } 1$ |
| L         | H  | H  | L  |  | $F = A \oplus B$       | $F = A \text{ MINUS } B \text{ MINUS } 1$ | $F = A \text{ MINUS } B$                                  |
| L         | H  | H  | H  |  | $F = A\overline{B}$    | $F = \overline{AB} \text{ MINUS } 1$      | $F = A\overline{B}$                                       |
| H         | L  | L  | L  |  | $F = \overline{A + B}$ | $F = A \text{ PLUS } AB$                  | $F = A \text{ PLUS } AB \text{ PLUS } 1$                  |
| H         | L  | L  | H  |  | $F = A \oplus B$       | $F = A \text{ PLUS } B$                   | $F = A \text{ PLUS } B \text{ PLUS } 1$                   |
| H         | L  | H  | L  |  | $F = B$                | $F = (A + \overline{B}) \text{ PLUS } AB$ | $F = (A + \overline{B}) \text{ PLUS } AB \text{ PLUS } 1$ |
| H         | L  | H  | H  |  | $F = AB$               | $F = AB \text{ MINUS } 1$                 | $F = AB$                                                  |
| H         | H  | L  | L  |  | $F = 1$                | $F = A$                                   | $F = A \text{ PLUS } A \text{ PLUS } 1$                   |
| H         | H  | L  | H  |  | $F = A + \overline{B}$ | $F = (A + B) \text{ PLUS } A$             | $F = (A + B) \text{ PLUS } A \text{ PLUS } 1$             |
| H         | H  | H  | L  |  | $F = A + B$            | $F = (A + \overline{B}) \text{ PLUS } A$  | $F = (A + \overline{B}) \text{ PLUS } A \text{ PLUS } 1$  |
| H         | H  | H  | H  |  | $F = A$                | $F = A \text{ MINUS } 1$                  | $F = A$                                                   |

TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181  
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram



Pin numbers shown on logic notation are for DW, J or N packages.

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TTL DEVICES

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3-713

# TYPES SN54181, SN74181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                               |                |
|-----------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)         | 7 V            |
| Input voltage                                 | 5.5 V          |
| Interemitter voltage (see Note 2)             | 5.5 V          |
| Operating free-air temperature range: SN54181 | -55°C to 125°C |
| SN74181                                       | 0°C to 70°C    |
| Storage temperature range                     | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each  $\bar{A}$  input in conjunction with inputs S2 or S3, and to each  $\bar{B}$  input in conjunction with inputs S0 or S3.

## recommended operating conditions

|                                                                | SN54181 |     |      | SN74181 |     |      | UNIT    |
|----------------------------------------------------------------|---------|-----|------|---------|-----|------|---------|
|                                                                | MIN     | NOM | MAX  | MIN     | NOM | MAX  |         |
| Supply voltage, $V_{CC}$                                       | 4.5     | 5   | 5.5  | 4.75    | 5   | 5.25 | V       |
| High-level output current, $I_{OH}$ (All outputs except A = B) |         |     | -800 |         |     | -800 | $\mu$ A |
| Low-level output current, $I_{OL}$                             |         |     | 16   |         |     | 16   | mA      |
| Operating free-air temperature, $T_A$                          | -55     |     | 125  | 0       |     | 70   | °C      |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                                         | TEST CONDITIONS†                                                                               | SN54181 |      |      | SN74181 |      |      | UNIT    |
|-----------|---------------------------------------------------------|------------------------------------------------------------------------------------------------|---------|------|------|---------|------|------|---------|
|           |                                                         |                                                                                                | MIN     | TYP‡ | MAX  | MIN     | TYP‡ | MAX  |         |
| $V_{IH}$  | High-level input voltage                                |                                                                                                | 2       |      |      | 2       |      |      | V       |
| $V_{IL}$  | Low-level input voltage                                 |                                                                                                |         |      | 0.8  |         |      | 0.8  | V       |
| $V_{IK}$  | Input clamp voltage                                     | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$                                                    |         |      | -1.5 |         |      | -1.5 | V       |
| $V_{OH}$  | High-level output voltage, any output except A = B      | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$ | 2.4     | 3.4  |      | 2.4     | 3.4  |      | V       |
| $I_{OH}$  | High-level output current, A = B output only            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$    |         |      | 250  |         |      | 250  | $\mu$ A |
| $V_{OL}$  | Low-level output voltage                                | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$    |         | 0.2  | 0.4  |         | 0.2  | 0.4  | V       |
| $I_I$     | Input current at maximum input voltage                  | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                     |         |      | 1    |         |      | 1    | mA      |
| $I_{IH}$  | High-level input current                                | Mode input                                                                                     |         |      | 40   |         |      | 40   | $\mu$ A |
|           |                                                         | Any $\bar{A}$ or $\bar{B}$ input                                                               |         |      | 120  |         |      | 120  |         |
|           |                                                         | Any S input                                                                                    |         |      | 160  |         |      | 160  |         |
|           |                                                         | Carry input                                                                                    |         |      | 200  |         |      | 200  |         |
| $I_{IL}$  | Low-level input current                                 | Mode input                                                                                     |         |      | -1.6 |         |      | -1.6 | mA      |
|           |                                                         | Any $\bar{A}$ or $\bar{B}$ input                                                               |         |      | -4.8 |         |      | -4.8 |         |
|           |                                                         | Any S input                                                                                    |         |      | -6.4 |         |      | -6.4 |         |
|           |                                                         | Carry input                                                                                    |         |      | -8   |         |      | -8   |         |
| $I_{OS}$  | Short-circuit output current, any output except A = B § | $V_{CC} = \text{MAX}$                                                                          | -20     |      | -55  | -18     |      | -57  | mA      |
| $I_{CC}$  | Supply current                                          | $V_{CC} = \text{MAX},$ Condition A                                                             | 88      | 127  |      | 88      | 140  |      | mA      |
|           |                                                         | See Note 3, Condition B                                                                        | 94      | 135  |      | 94      | 150  |      | mA      |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time.

NOTE 3: With outputs open,  $I_{CC}$  is measured for the following conditions:

A. S0 through S3, M, and  $\bar{A}$  inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

# TYPES SN54181, SN74181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  ( $C_L = 15\text{ pF}$ ,  $R_L = 400\ \Omega$ , see note 4)

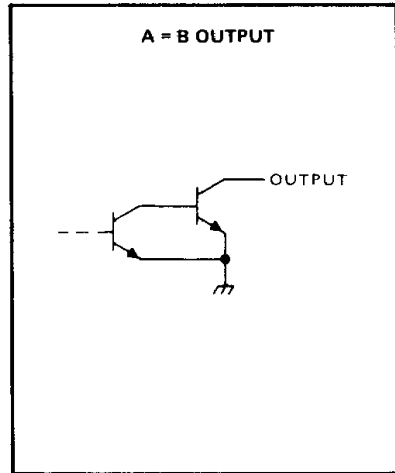
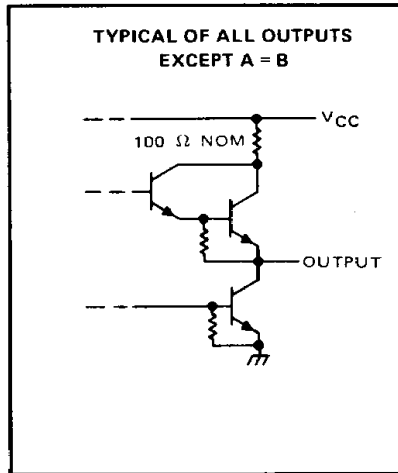
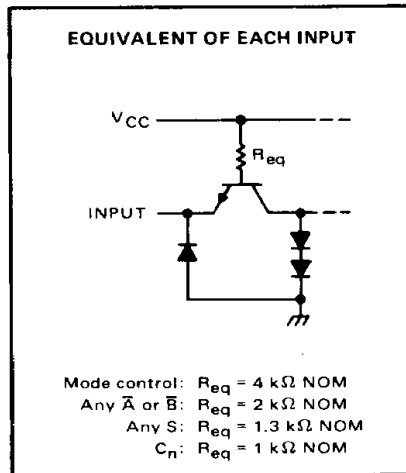
| PARAMETER <sup>†</sup> | FROM (INPUT)                         | TO (OUTPUT)        | TEST CONDITIONS                                        | MIN | TYP | MAX | UNIT |
|------------------------|--------------------------------------|--------------------|--------------------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub>       | C <sub>n</sub>                       | C <sub>n+4</sub>   |                                                        | 12  | 18  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 13  | 19  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | C <sub>n+4</sub>   | M = 0 V, S0 = S3 = 4.5 V,<br>S1 = S2 = 0 V (SUM mode)  | 28  | 43  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 27  | 41  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | C <sub>n+4</sub>   | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 35  | 50  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 33  | 50  |     |      |
| t <sub>PLH</sub>       | C <sub>n</sub>                       | Any $\overline{F}$ | M = 0 V<br>(SUM or DIFF mode)                          | 13  | 19  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 12  | 18  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | $\overline{G}$     | M = 0 V, S0 = S3 = 4.5 V,<br>S1 = S2 = 0 V (SUM mode)  | 13  | 19  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 13  | 19  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | $\overline{G}$     | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 17  | 25  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 17  | 25  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | $\overline{P}$     | M = 0 V, S0 = S3 = 4.5 V,<br>S1 = S2 = 0 V (SUM mode)  | 13  | 19  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 17  | 25  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | $\overline{P}$     | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 17  | 25  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 17  | 25  |     |      |
| t <sub>PLH</sub>       | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$   | M = 0 V, S0 = S3 = 4.5 V,<br>S1 = S2 = 0 V (SUM mode)  | 28  | 42  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 21  | 32  |     |      |
| t <sub>PLH</sub>       | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$   | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 32  | 48  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 23  | 34  |     |      |
| t <sub>PLH</sub>       | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$   | M = 4.5 V (logic mode)                                 | 32  | 48  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 23  | 34  |     |      |
| t <sub>PLH</sub>       | Any $\overline{A}$ or $\overline{B}$ | A = B              | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 35  | 50  | ns  |      |
| t <sub>PHL</sub>       |                                      |                    |                                                        | 32  | 48  |     |      |

<sup>†</sup>  $t_{PLH}$   $\equiv$  propagation delay time, low-to-high-level output

$t_{PHL}$   $\equiv$  propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

## schematics of inputs and outputs



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TTL DEVICES

**TEXAS  
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# TYPES SN54LS181, SN74LS181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage                                   | 5.5 V          |
| Intermitter voltage (see Note 2)                | 5.5 V          |
| Operating free-air temperature range: SN54LS181 | −55°C to 125°C |
| SN74LS181                                       | 0°C to 70°C    |
| Storage temperature range                       | −65°C to 150°C |

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each  $\bar{A}$  input in conjunction with inputs S2 or S3, and to each  $\bar{B}$  input in conjunction with inputs S0 or S3.

## recommended operating conditions

|                                                                | SN54LS181 |     |      | SN74LS181 |     |      | UNIT    |
|----------------------------------------------------------------|-----------|-----|------|-----------|-----|------|---------|
|                                                                | MIN       | NOM | MAX  | MIN       | NOM | MAX  |         |
| Supply voltage, $V_{CC}$                                       | 4.5       | 5   | 5.5  | 4.75      | 5   | 5.25 | V       |
| High-level output current, $I_{OH}$ (All outputs except A = B) |           |     | −400 |           |     | −400 | $\mu$ A |
| Low-level output current, $I_{OL}$                             |           |     | 4    |           |     | 8    | mA      |
| Operating free-air temperature, $T_A$                          | −55       |     | 125  | 0         |     | 70   | °C      |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                                         |                                  | TEST CONDITIONS†                                                                                    |                         | SN54LS181   |      |      | SN74LS181 |      |               | UNIT          |
|-----------|---------------------------------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------------|-------------------------|-------------|------|------|-----------|------|---------------|---------------|
|           |                                                         |                                  |                                                                                                     |                         | MIN         | TYP‡ | MAX  | MIN       | TYP‡ | MAX           |               |
| $V_{IH}$  | High-level input voltage                                |                                  |                                                                                                     |                         | 2           |      |      | 2         |      |               | V             |
| $V_{IL}$  | Low-level input voltage                                 |                                  |                                                                                                     |                         |             |      | 0.7  |           |      | 0.8           | V             |
| $V_{IK}$  | Input clamp voltage                                     |                                  | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                         |                         |             |      | -1.5 |           |      | -1.5          | V             |
| $V_{OH}$  | High-level output voltage, any output except A = B      |                                  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$ |                         | 2.5         | 3.4  |      | 2.7       | 3.4  |               | V             |
| $I_{OH}$  | High-level output current, A = B output only            |                                  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, V_{OH} = 5.5 \text{ V}$    |                         |             |      | 100  |           |      | 100           | $\mu\text{A}$ |
| $V_{OL}$  | Low-level output voltage                                | All outputs                      | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}$                            | $I_{OL} = 4 \text{ mA}$ | 0.25        | 0.4  |      | 0.25      | 0.4  | V             |               |
|           |                                                         | $I_{OL} = 8 \text{ mA}$          |                                                                                                     |                         |             |      | 0.35 | 0.5       |      |               |               |
|           |                                                         | $I_{OL} = 16 \text{ mA}$         |                                                                                                     | 0.47                    | 0.7         |      | 0.47 | 0.7       |      |               |               |
|           |                                                         | $I_{OL} = 8 \text{ mA}$          |                                                                                                     | 0.35                    | 0.6         |      | 0.35 | 0.5       |      |               |               |
| $I_I$     | Input current at max. input voltage                     | Mode input                       | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                          |                         |             |      | 0.1  |           | 0.1  | mA            |               |
|           |                                                         | Any $\bar{A}$ or $\bar{B}$ input |                                                                                                     |                         |             |      | 0.3  |           | 0.3  |               |               |
|           |                                                         | Any S input                      |                                                                                                     |                         |             |      | 0.4  |           | 0.4  |               |               |
|           |                                                         | Carry input                      |                                                                                                     |                         |             |      | 0.5  |           | 0.5  |               |               |
| $I_{IH}$  | High-level input current                                | Mode input                       | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                                          |                         |             |      | 20   |           | 20   | $\mu\text{A}$ |               |
|           |                                                         | Any $\bar{A}$ or $\bar{B}$ input |                                                                                                     |                         |             |      | 60   |           | 60   |               |               |
|           |                                                         | Any S input                      |                                                                                                     |                         |             |      | 80   |           | 80   |               |               |
|           |                                                         | Carry input                      |                                                                                                     |                         |             |      | 100  |           | 100  |               |               |
| $I_{IL}$  | Low-level input current                                 | Mode input                       | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                          |                         |             |      | -0.4 |           | -0.4 | mA            |               |
|           |                                                         | Any $\bar{A}$ or $\bar{B}$ input |                                                                                                     |                         |             |      | -1.2 |           | -1.2 |               |               |
|           |                                                         | Any S input                      |                                                                                                     |                         |             |      | -1.6 |           | -1.6 |               |               |
|           |                                                         | Carry input                      |                                                                                                     |                         |             |      | -2   |           | -2   |               |               |
| $I_{OS}$  | Short-circuit output current, any output except A = B § |                                  | $V_{CC} = \text{MAX}$                                                                               |                         | -6          |      | -40  | -5        |      | -42           | mA            |
| $I_{CC}$  | Supply current                                          |                                  | $V_{CC} = \text{MAX},$ See Note 3                                                                   |                         | Condition A | 20   | 32   |           | 20   | 34            | mA            |
|           |                                                         |                                  |                                                                                                     |                         | Condition B |      | 21   | 35        |      | 21            |               |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 3: With outputs open,  $I_{CC}$  is measured for the following conditions:

A. S0 through S3, M, and  $\bar{A}$  inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

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# TYPES SN54LS181, SN74LS181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , ( $C_L = 15\text{ pF}$ ,  $R_L = 2\text{ k}\Omega$ , see note 4)

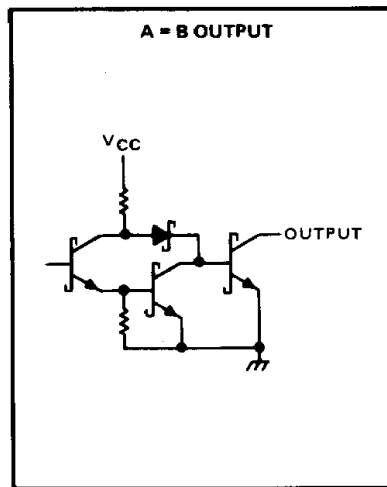
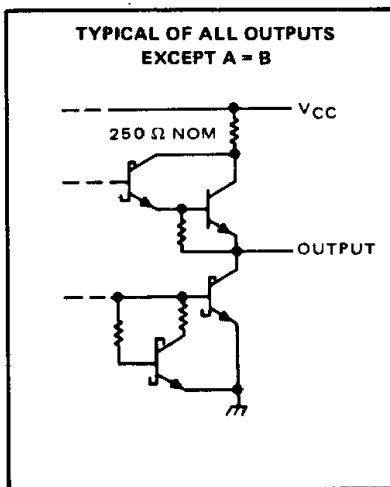
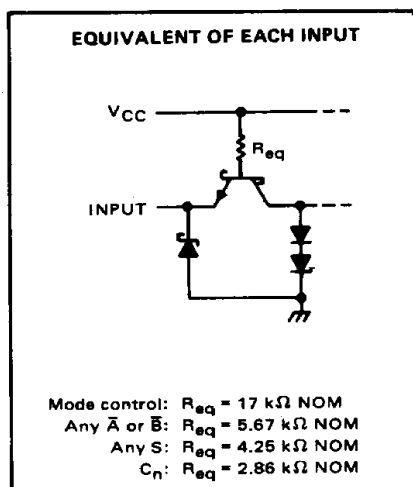
| PARAMETER <sup>†</sup> | FROM<br>(INPUT)            | TO<br>(OUTPUT) | TEST CONDITIONS                                                                     | MIN | TYP | MAX | UNIT |
|------------------------|----------------------------|----------------|-------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$              | $C_n$                      | $C_{n+4}$      |                                                                                     | 18  | 27  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 13  | 20  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $C_{n+4}$      | $M = 0\text{ V}, S_0 = S_3 = 4.5\text{ V},$<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  | 25  | 38  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 25  | 38  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $C_{n+4}$      | $M = 0\text{ V}, S_0 = S_3 = 0\text{ V}$<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)  | 27  | 41  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 27  | 41  |     |      |
| $t_{PLH}$              | $C_n$                      | Any $\bar{F}$  | $M = 0\text{ V}$<br>(SUM or DIFF mode)                                              | 17  | 26  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 13  | 20  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$      | $M = 0\text{ V}, S_0 = S_3 = 4.5\text{ V},$<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  | 19  | 29  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 15  | 23  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$      | $M = 0\text{ V}, S_0 = S_3 = 0\text{ V},$<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 21  | 32  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 21  | 32  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$      | $M = 0\text{ V}, S_0 = S_3 = 4.5\text{ V},$<br>$S_1 = S_2 = 0\text{ V},$ (SUM mode) | 20  | 30  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 20  | 30  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$      | $M = 0\text{ V}, S_0 = S_3 = 0\text{ V},$<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 20  | 30  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 22  | 33  |     |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$    | $M = 0\text{ V}, S_0 = S_3 = 4.5\text{ V},$<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  | 21  | 32  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 13  | 20  |     |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$    | $M = 0\text{ V}, S_0 = S_3 = 0\text{ V},$<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 21  | 32  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 21  | 32  |     |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$    | $M = 4.5\text{ V}$ (logic mode)                                                     | 22  | 33  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 26  | 38  |     |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $A = B$        | $M = 0\text{ V}, S_0 = S_3 = 0\text{ V},$<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 33  | 50  | ns  |      |
| $t_{PHL}$              |                            |                |                                                                                     | 41  | 62  |     |      |

<sup>†</sup> $t_{PLH}$   $\equiv$  propagation delay time, low-to-high-level output

$t_{PHL}$   $\equiv$  propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

## schematics of inputs and outputs



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TTL DEVICES

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# TYPES SN54S181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                          |                |
|------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)    | 7 V            |
| Input voltage                            | 5.5 V          |
| Interemitter voltage (see Note 2)        | 5.5 V          |
| Operating free-air temperature: SN54S181 | -55°C to 125°C |
| SN74S181                                 | 0°C to 70°C    |
| Storage temperature range                | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each  $\bar{A}$  input in conjunction with inputs S2 or S3, and to each  $\bar{B}$  input in conjunction with inputs S0 or S3.

## recommended operating conditions

|                                                                | SN54S181 |     |     | SN74S181 |     |      | UNIT |
|----------------------------------------------------------------|----------|-----|-----|----------|-----|------|------|
|                                                                | MIN      | NOM | MAX | MIN      | NOM | MAX  |      |
| Supply voltage, $V_{CC}$                                       | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V    |
| High-level output current, $I_{OH}$ (All outputs except A = B) |          |     | -1  |          |     | -1   | mA   |
| Low-level output current, $I_{OL}$                             |          |     | 20  |          |     | 20   | mA   |
| Operating free-air temperature, $T_A$                          | -55      |     | 125 | 0        |     | 70   | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                                         | TEST CONDITIONS†                                                                                                           | SN54S181 |      |         | SN74S181 |      |         | UNIT |
|-----------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|----------|------|---------|----------|------|---------|------|
|           |                                                         |                                                                                                                            | MIN      | TYP‡ | MAX     | MIN      | TYP‡ | MAX     |      |
| $V_{IH}$  | High-level input voltage                                |                                                                                                                            | 2        |      |         | 2        |      |         | V    |
| $V_{IL}$  | Low-level input voltage                                 |                                                                                                                            |          |      | 0.8     |          |      | 0.8     | V    |
| $V_{IK}$  | Input clamp voltage                                     | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                                                |          |      | -1.2    |          |      | -1.2    | V    |
| $V_{OH}$  | High-level output voltage, any output except A = B      | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$                                | 2.5      | 3.4  |         | 2.7      | 3.4  |         | V    |
| $I_{OH}$  | High-level output current, A = B output only            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$                                |          |      | 250     |          |      | 250     | µA   |
| $V_{OL}$  | Low-level output voltage                                | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$                                |          |      | 0.5     |          |      | 0.5     | V    |
| $I_I$     | Input current at maximum input voltage                  | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                                                 |          |      | 1       |          |      | 1       | mA   |
| $I_{IH}$  | High-level input current                                | Mode input<br>Any $\bar{A}$ or $\bar{B}$ input<br>Any S input<br>Carry input<br>$V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$ |          |      | 50      |          |      | 50      | µA   |
|           |                                                         |                                                                                                                            |          |      | 150     |          |      | 150     |      |
|           |                                                         |                                                                                                                            |          |      | 200     |          |      | 200     |      |
|           |                                                         |                                                                                                                            |          |      | 250     |          |      | 250     |      |
| $I_{IL}$  | Low-level input current                                 | Mode input<br>Any $\bar{A}$ or $\bar{B}$ input<br>Any S input<br>Carry input<br>$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ |          |      | -2      |          |      | -2      | mA   |
|           |                                                         |                                                                                                                            |          |      | -6      |          |      | -6      |      |
|           |                                                         |                                                                                                                            |          |      | -8      |          |      | -8      |      |
|           |                                                         |                                                                                                                            |          |      | -10     |          |      | -10     |      |
| $I_{OS}$  | Short-circuit output current, any output except A = B § | $V_{CC} = \text{MAX}$                                                                                                      | -40      |      | -100    | -40      |      | -100    | mA   |
| $I_{CC}$  | Supply current                                          | $V_{CC} = \text{MAX}, T_A = 125^\circ\text{C},$ W package only                                                             |          |      | 195     |          |      |         | mA   |
|           |                                                         | See Note 3<br>$V_{CC} = \text{MAX},$ See Note 3 All packages                                                               |          |      | 120 220 |          |      | 120 220 |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 3:  $I_{CC}$  is measured for the following conditions (the typical and maximum values apply to both):

- A. S0 through S3, M, and  $\bar{A}$  inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.
- B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.

# TYPES SN54S181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  ( $C_L = 15\text{ pF}$ ,  $R_L = 280\ \Omega$ , see note 4)

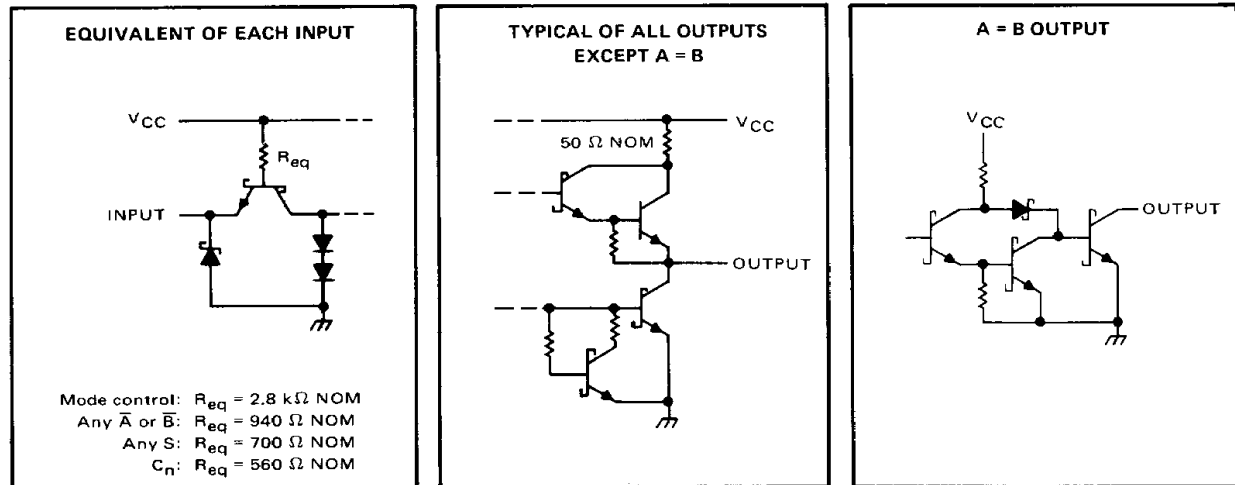
| PARAMETER <sup>1</sup> | FROM (INPUT)               | TO (OUTPUT)   | TEST CONDITIONS                                                                         | MIN | TYP  | MAX  | UNIT |
|------------------------|----------------------------|---------------|-----------------------------------------------------------------------------------------|-----|------|------|------|
| $t_{PLH}$              | $C_n$                      | $C_{n+4}$     |                                                                                         |     | 7    | 10.5 | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 7    | 10.5 |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $C_{n+4}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ ,<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  |     | 12.5 | 18.5 | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 12.5 | 18.5 |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $C_{n+4}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ ,<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) |     | 15.5 | 23   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 15.5 | 23   |      |
| $t_{PLH}$              | $C_n$                      | Any $\bar{F}$ | $M = 0\text{ V}$<br>(SUM or DIFF mode)                                                  |     | 7    | 12   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 7    | 12   |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ ,<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  |     | 8    | 12   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 7.5  | 12   |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ ,<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) |     | 10.5 | 15   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 10.5 | 15   |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ ,<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  |     | 7.5  | 12   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 7.5  | 12   |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$     | $M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ ,<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) |     | 10.5 | 15   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 10.5 | 15   |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$   | $M = 0\text{ V}$ , $S_0 = S_3 = 4.5\text{ V}$ ,<br>$S_1 = S_2 = 0\text{ V}$ (SUM mode)  |     | 11   | 16.5 | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 11   | 16.5 |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $F_i$         | $M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ ,<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) |     | 14   | 20   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 14   | 22   |      |
| $t_{PLH}$              | $\bar{A}_i$ or $\bar{B}_i$ | $F_i$         | $M = 4.5\text{ V}$ (logic mode)                                                         |     | 14   | 20   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 14   | 22   |      |
| $t_{PLH}$              | Any $\bar{A}$ or $\bar{B}$ | $A = B$       | $M = 0\text{ V}$ , $S_0 = S_3 = 0\text{ V}$ ,<br>$S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) |     | 15   | 23   | ns   |
| $t_{PHL}$              |                            |               |                                                                                         |     | 20   | 30   |      |

<sup>1</sup>  $t_{PLH}$   $\equiv$  propagation delay time, low-to-high-level output

$t_{PHL}$   $\equiv$  propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

## schematics of inputs and outputs



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TTL DEVICES

**TEXAS  
INSTRUMENTS**

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# TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## PARAMETER MEASUREMENT INFORMATION

### SUM MODE TEST TABLE

FUNCTION INPUTS:  $S_0 = S_3 = 4.5 \text{ V}$ ,  $S_1 = S_2 = M = 0 \text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS                 |                                           | OUTPUT UNDER TEST    | OUTPUT WAVEFORM (See Note 4) |
|-----------|------------------|----------------------|-------------|-----------------------------------|-------------------------------------------|----------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                       | APPLY GND                                 |                      |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$          | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$          | In-Phase                     |
| $t_{PLH}$ | $A_i$            | $B_i$                | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $P$                  | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $P$                  | In-Phase                     |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$            | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$            | In-Phase                     |
| $t_{PLH}$ | $C_n$            | None                 | None        | All $\bar{A}$                     | All $\bar{B}$                             | Any $F$ or $C_{n+4}$ | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_{n+4}$            | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_{n+4}$            | Out-of-Phase                 |

### DIFF MODE TEST TABLE

FUNCTION INPUTS:  $S_1 = S_2 = 4.5 \text{ V}$ ,  $S_0 = S_3 = M = 0 \text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS           |                                           | OUTPUT UNDER TEST    | OUTPUT WAVEFORM (See Note 4) |
|-----------|------------------|----------------------|-------------|-----------------------------|-------------------------------------------|----------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                 | APPLY GND                                 |                      |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$          | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | $A_i$                | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$          | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $P$                  | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $P$                  | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$            | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$            | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$              | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$              | Out-of-Phase                 |
| $t_{PLH}$ | $C_n$            | None                 | None        | All $\bar{A}$ and $\bar{B}$ | None                                      | $C_{n+4}$ or any $F$ | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_{n+4}$            | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_{n+4}$            | In-Phase                     |

### LOGIC MODE TEST TABLE

FUNCTION INPUTS:  $S_1 = S_2 = M = 4.5 \text{ V}$ ,  $S_0 = S_3 = 0 \text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |           | OTHER DATA INPUTS |                                           | OUTPUT UNDER TEST | OUTPUT WAVEFORM (See Note 4) |
|-----------|------------------|----------------------|-----------|-------------------|-------------------------------------------|-------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND | APPLY 4.5 V       | APPLY GND                                 |                   |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{F}_i$       | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{F}_i$       | Out-of-Phase                 |

NOTE 4: See General Information Section for load circuits and voltage waveforms

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